REMARKS

Summary of the Office Action

Claims 5-6 and 18-20 stand rejected under 35 U.S.C. § 102(a) as being anticipated by *Nanno et al.* (U.S. Patent 6,909,413), which is equivalent to WO02/35507. Claims 1-4, 7-11, and 13-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Owaku et al.* (JP 10-232652) in view of *Isozaki* (U.S. Patent 5,576,737). Claims 12 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Owaku et al.* in view of *Isozaki*, and further in view of *Ishiyama* (U.S. Publication 2003/0053321).

Summary of the Response to the Office Action

Applicants have amended claims 5 and 18. Accordingly, claims 1-21 are pending for further consideration.

The Rejection Under 35 U.S.C. § 102(a)

Claims 5-6 and 18-20 stand rejected under 35 U.S.C. § 102(a) as being anticipated by *Nanno et al.* (U.S. Patent 6,909,413), which is equivalent to WO02/35507. Applicants respectfully traverse the rejection for at least the following reasons.

Independent claim 5, as amended, recites "supplying the power source voltage to digital circuit devices including an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signal, wherein the interface circuit includes a low voltage differential signaling receiver which lowers a voltage level of the signals input from the system to thereby reduce the number of signal lines needed to the system and the timing controller," (emphasis added). In contrast, FIG. 9 of *Nanno et al.* merely discloses a power supply circuit 24

supplying a power source to the source driver circuit 22A, gate driver circuit 21, and a driver circuit applying compensation voltage 23.

The Final Office Action suggests that the power supply 24 of *Nanno et al.* is the interface circuit, as claimed. Applicants respectfully assert that *Nanno et al.* is silent as to supplying a power source to an interface circuit, a timing controller, and a data driving circuit, wherein the interface circuit includes a low voltage differential signaling receiver which lowers a voltage level of the signals input from the system to thereby reduce the number of signal lines needed to the system and the timing controller, as required by independent claim 5, as amended.

In addition, the Final Office Action suggests that the start pulse circuits and transfer clock circuits embedded into data and gate drivers (col. 7, lines 40-54 of *Nanno et al.*) are timing circuits. Applicants respectfully assert that col. 7, lines 40-54 of *Nanno et al.* is still completely silent as to a timing controller. Therefore, Applicants respectfully assert that the rejection under 35 U.S.C. § 102(a) should be withdrawn because *Nanno et al.* does not teach or suggest each feature of independent claim 5. As pointed out in MPEP § 2131, "[t]o anticipate a claim, the reference must teach every element of the claim." Thus, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Verdegaal Bros. v. Union Oil Co. Of California, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987)." Furthermore, Applicants respectfully assert that independent claim 18 is allowable for similar reasons and that dependent claims 6, 19, and 20 are allowable at least because of their dependence from the independent claims.

The Rejection Under 35 U.S.C. § 103(a) and Withdrawal of Finality

Claims 1-4, 7-11, and 13-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Owaku et al.* (JP 10-232652) in view of *Isozaki* (U.S. Patent 5,576,737). Claims 12 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Owaku et al.* in view of *Isozaki*, and further in view of *Ishiyama* (U.S. Publication 2003/0053321). Applicants respectfully traverse the rejection for at least the following reasons.

The Final Office Action alleges that *Owaku et al.* teaches supplying a power source voltage 3.3V to a display processing circuitry 20 from the system 10, and that *Isozaki* teaches that such circuitry may include components that require lower operating voltage, for example 2.7V. Applicants respectfully assert that the Final Office Action has incorrectly pieced together two references to teach the claimed features.

MPEP § 2143.01 instructs that "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ 2d 1430 (Fed. Cir. 1990)." MPEP § 2143.01 further instructs that "[a]lthough a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so.'" Applicants respectfully submit that the references alleged by the Final Office Action do not provide such a suggestion or motivation.

Even if the references do provide such a suggestion or motivation, Applicants respectfully assert that *Owaku et al.* and *Isozaki* fail to disclose the features including "reducing a power source voltage from a system" and "supplying the reduced power source voltage to digital

circuit devices for processing digital signal," as required by independent claim 1. The second paragraph of page 4 of the Final Office Action admits that *Owaku et al.* fails to disclose the step of reducing the power source voltage from the system. Accordingly, *Owaku et al.* also fails to disclose the step of supplying the reduced power source voltage from a system to digital circuit devices. However, the Final Office Action alleges that *Owaku et al.* teaches supplying a power source voltage 3.3V to a display processing circuitry 20 from the system 10, and that of *Isozaki* teaches that "such circuitry" may include components that require lower operating voltage, for example 2.7V. Applicants respectfully assert that "such circuitry" fails to include the features of "reducing the power source voltage from the system." Applicants respectfully assert that "using a reduced voltage" is completely unrelated to "reducing the power source voltage."

In addition, Applicants respectfully assert that the Examiner has failed to address Applicants' arguments presented in the Amendment filed on September 20, 2006, although the prior art rejections have been maintained in the Final Office Action. Specifically, the Examiner has failed to rebut Applicants' arguments directed toward the features including "reducing a power source voltage from a system" and "supplying the reduced power source voltage to digital circuit devices for processing digital signal," as required by independent claim 1, which are allegedly disclosed by *Isozaki.*

As directed by MPEP 707.07(f), "[w]here the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument **and answer the substance of it**" (emphasis added). Accordingly, Applicants respectfully assert that the Examiner has not addressed Applicants' arguments set forth in the Amendment filed on

September 20, 2006. Thus, Applicants further assert that the finality of the Final Office Action dated December 12, 2006, should be withdrawn in order for Applicants to receive answers to the arguments set forth in their Amendment filed on September 20, 2006, and reiterated below.

Independent claim 1 recites, in part, "reducing a power source voltage from a system and supplying the reduced power source voltage to digital circuit devices for processing digital signal," (emphasis added). In contrast, the Office Action admits that *Owaku et al.* fails to disclose supplying a power source voltage from a system to digital circuit devices. Furthermore, *Isozaki* merely discloses using a voltage with a low magnitude (-2.7V) by setting V_{DD} to 0V and V_{as} to -2.7V (See col. 10, line 21).

The Office Action then merely makes a somewhat dismissive statement that the voltage "needs to be reduced by any known in the art methods." It is not clear whether the Final Office Action is taking official notice that "reducing power source voltage from a system" and "supplying the reduced power source voltage to digital circuit devices for processing digital signal" are known to those skilled in the art. If so, Applicants respectfully assert that the notice is in error and request that the Office produce authority for the statement pursuant to MPEP § 2144.03(c). Otherwise, Applicants respectfully assert that *Owaku et al.* and *Isozaki* fail to disclose, either singly or in combination, both "reducing a power source voltage from a system" and "supplying the reduced power source voltage to digital circuit devices for processing digital signal," as required by independent claim 1.

Therefore, Applicants respectfully assert that the rejection under 103(a) should be withdrawn because *Owaku et al.*, *Isozaki* and *Ishiyama*, whether taken singly or combined, do

not teach or suggest each feature of independent claim 1. MPEP § 2143.03 instructs that "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 409 F.2d 981, 180 USPQ 580 (CCPA 1974)." Furthermore, Applicants respectfully assert that independent claim 7 is allowable for similar reasons and that dependent claims 2-4, 8-17, and 21 are allowable at least because of their dependence from the independent claims.

Conclusion

In view of the foregoing, Applicants respectfully request reconsideration and the timely allowance of all pending claims. Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicants' undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310.

Respectfully submitted,

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